

REMARKS / DISCUSSION OF ISSUES

In the Examiner's Answer, the Examiner noted that Claim 4 had minor errors. These minor errors have been corrected and revised claim list including an amended Claim 4 is submitted herewith.

Appellant maintains the arguments submitted in the Appeal Brief filed on November 13, 2006, which are incorporated herein by reference. Further, Appellant refutes the allegations made in the Examiner's Answer of May 4, 2007.

In particular, Appellant respectfully refutes the allegation on page 4 of the Examiner's Answer that FIG 3b, element 117 of Miller, as well as column 6, lines 31-35 and lines 53-58 disclose at least one instruction comprising particular information inserted at compile time (where the particular information inserted at compile time signals explicitly how the processing unit, when processing the instruction from a current memory line, should control how a part of processing is affected by crossing of a boundary to a subsequent memory line), as recited in independent Claims 1 and 8.

It is respectfully submitted that element 117 of Miller, namely an end-of-packet (EP), not-end-of-packet (NEP), or a stop bit, is not equivalent to information that "signals explicitly how the processing unit, when processing the instruction from a current memory line, should control how a part of processing is affected by crossing of a boundary to a subsequent memory line," as required by independent Claims 1 and 8.

Assuming, arguendo, that Miller teaches information that signals explicitly how a processing unit should control how a part of processing is affected by crossing of a boundary to a subsequent memory line, it is respectfully submitted that Miller does not disclose or suggest that such information is inserted at compile time, as required by independent Claims 1 and 8. Rather, any such information is already present in the Miller memory, where the Miller processor merely compresses and processes such information.

Such information inserted at compile time is nowhere taught or suggested in Miller. Element 117 of Miller shown in FIG 3b, is merely an end-of-packet (EP) or

not-end-of-packet (NEP) field that permits the Miller system "to determine whether the particular compressed instruction is at the end of a compressed instruction packet, and performs the same function as the stop bit 113 in the 16 bit long compressed instruction." (Column 6, lines 32-35, emphasis added)

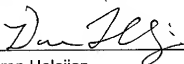
FIG 4 of Miller shows an uncompressed very long instruction word (VLIW) 120, and a corresponding compressed instruction packet 121. As clearly shown in FIG 4, the "stop bit 128 and the control bits 130 of the uncompressed instruction are compressed into the 6 bit stop bit and token field 132, 134." (Column 7, lines 22-23, emphasis added) That is, the stop bit is already present in the uncompressed instruction and is merely compressed. Miller simply does not teach or suggest that the stop bit or an EP/NEP is inserted at compile time.

In stark contrast, the present invention as recited in independent Claims 1 and 8, amongst other patentable elements, requires that the at least one instruction comprising information is inserted at compile time, where the information signals explicitly how the processing unit, when processing the instruction from a current memory line, should control how a part of processing is affected by crossing of a boundary to a subsequent memory line.

Accordingly, it is respectfully submitted that independent Claims 1 and 8 are allowable, and allowance thereof is respectfully requested. In addition, it is respectfully submitted that Claims 2-7 and 9 should also be allowed at least based on their dependence from independent Claim 1 and 8, as well as for the separately patentable elements contained in each of the dependent claims.

In view of the foregoing, Appellant respectfully submits the rejection of Claims 1-9 should be reversed.

Respectfully submitted,



Dicran Halajian  
Reg. 39,703  
Attorney for Appellant  
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**THORNE & HALAJIAN, LLP**  
Applied Technology Center  
111 West Main Street  
Bay Shore, NY 11706  
Phone: (631) 665-5139  
Fax: (631) 665-5101